AiP74HC/HCT4097
Dual 8-channel Analog Multiplexer/Demultiplexer

Product Specification

Specification Revision History:

Version	Date	Description
2019-12-A1	2019-12	New
2022-02-A2	2022-02	Modify Ordering Information
2023-11-A3	2023-11	Modify ambient temperature to -40℃~+125℃ and modify the ordering information

1、General Description

The AIP74HC/HCT4097 is a differential 8-channel multiplexer having three binary control inputs A0, A1, A2 and an inhibit input ($\overline{E}$). The inputs permit selection of one of eight pairs of switches. With $\overline{E}$ HIGH all switches are in the high-impedance OFF-state, independent of A0 to A2.

The analog inputs/outputs (nY0 to nY7 and nZ) can swing between V_{DD} as a positive limit and V_{SS} as a negative limit. V_{DD} to V_{SS} may not exceed 15V.

Features:

- Wide supply voltage range from 3V to 9V
- Fully static operation
- 5V and 9V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40℃ to +125℃
- Packaging information: SOP24/TSSOP24

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74HC4097SA24.TB	SOP24	74HC4097	30 PCS/tube	80 tube/box	2400 PCS/box	Dimensions of plastic enclosure: 15.4mm×7.5mm Pin spacing: 1.27mm
AiP74HCT4097SA24.TB	SOP24	74HCT4097	30 PCS/tube	80 tube/box	2400 PCS/box	Dimensions of plastic enclosure: 15.4mm×7.5mm Pin spacing: 1.27mm
AiP74HC4097TA24.TB	TSSOP24	74HC4097	62 PCS/tube	200 tube/box	12400 PCS/box	Dimensions of plastic enclosure: 7.8mm×4.4mm Pin spacing: 0.65mm
AiP74HCT4097TA24.TB	TSSOP24	74HCT4097	62 PCS/tube	200 tube/box	12400 PCS/box	Dimensions of plastic enclosure: 7.8mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74HC4097SA24.TR	SOP24	74HC4097	1250 PCS/reel	1250 PCS/box	Dimensions of plastic enclosure: 15.4mm×7.5mm Pin spacing:1.27mm
AiP74HCT4097SA24.TR	SOP24	74HCT4097	1250 PCS/reel	1250 PCS/box	Dimensions of plastic enclosure: 15.4mm×7.5mm Pin spacing:1.27mm
AiP74HC4097TA24.TR	TSSOP24	74HC4097	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 7.8mm×4.4mm Pin spacing:0.65mm
AiP74HCT4097TA24.TR	TSSOP24	74HCT4097	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 7.8mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

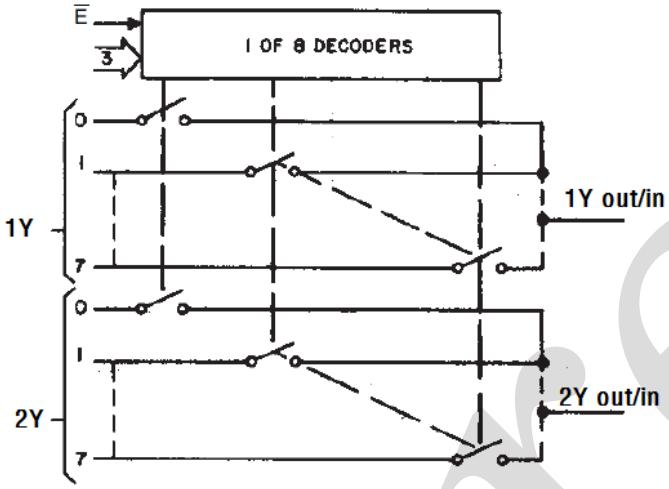
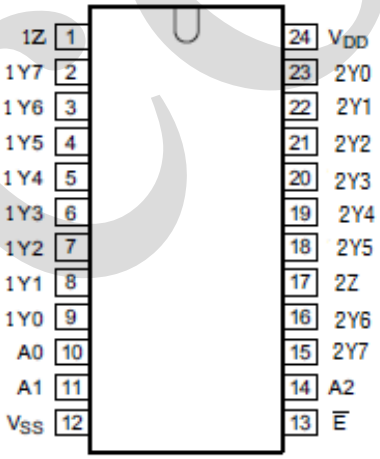


Figure 1. Functional diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	1Z	common input/output
2	1Y7	independent input/output
3	1Y6	independent input/output
4	1Y5	independent input/output
5	1Y4	independent input/output
6	1Y3	independent input/output
7	1Y2	independent input/output
8	1Y1	independent input/output
9	1Y0	independent input/output
10	A0	address input
11	A1	address input
12	V_{SS}	ground (0V)
13	$\overline{E}$	enable input (active LOW)
14	A2	address input
15	2Y7	independent input/output
16	2Y6	independent input/output
17	2Z	common input/output
18	2Y5	independent input/output
19	2Y4	independent input/output
20	2Y3	independent input/output
21	2Y2	independent input/output
22	2Y1	independent input/output
23	2Y0	independent input/output
24	V_{DD}	supply voltage

2.4、Function Table

Input				Selected Channel
$\overline{E}$	A2	A1	A0	
L	L	L	L	1Y0, 2Y0
L	L	L	H	1Y1, 2Y1
L	L	H	L	1Y2, 2Y2
L	L	H	H	1Y3, 2Y3
L	H	L	L	1Y4, 2Y4
L	H	L	H	1Y5, 2Y5
L	H	H	L	1Y6, 2Y6
L	H	H	H	1Y7, 2Y7
H	X	X	X	none

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{DD}	-[1]	-0.5	+11.0	V
input clamping current	I_{IK}	V_I<0.5V or V_I>V_{DD}+0.5V	-	±20	mA
switch clamping current	I_{SK}	V_{SW}<-0.5V or V_{SW}>V_{DD}+0.5V	-	±20	mA
switch current	I_{SW}	V_{SW}=-0.5V to V_{DD}+0.5V	-	±25	mA
supply current	I_{DD}	-	-	+50	mA
ground current	I_{SS}	-	-50	-	mA
storage temperature	T_{stg}	-	-65	+150	℃
total power dissipation	P_{tot}	-[2]	-	500	mW
device dissipation	P	per output transistor	-	100	mW
Soldering temperature	T_L	10s	260		℃

Note:

[1] To avoid drawing V_{DD} current out of terminal nZ, when switch current flows in terminals nYn, the voltage drop across the bidirectional switch must not exceed 0.4V. If the switch current flows into terminal nZ, no V_{DD} current will flow out of terminals nYn. In this case there is no limit for the voltage drop across the switch, but the voltages at nYn and nZ may not exceed V_{DD} or V_{SS}.

[2] For SOP24 packages: above 70℃ the value of P_{tot} derates linearly with 8mW/K.
For TSSOP24 packages: above 60℃ the value of P_{tot} derates linearly with 5.5mW/K.

3.2、Recommended Operating Conditions

(T_{amb}=25℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
AiP74HC4097						
supply voltage	V_{DD}	-	3.0	5.0	9.0	V
input voltage	V_I	-	V_{SS}	-	V_{DD}	V
switch voltage	V_{SW}	-	V_{SS}	-	V_{DD}	V
input transition rise and fall rate	Δt/ΔV	V_{DD}=4.5V	-	1.67	139	ns
		V_{DD}=6.0V	-	-	83	ns
		V_{DD}=9.0V	-	-	31	ns
ambient temperature	T_{amb}	in free air	-40	-	+125	℃
AiP74HCT4097						
supply voltage	V_{DD}	-	4.5	5.0	5.5	V
input voltage	V_I	-	V_{SS}	-	V_{DD}	V
switch voltage	V_{SW}	-	V_{SS}	-	V_{DD}	V
input transition rise and fall rate	Δt/ΔV	V_{DD}=4.5V	-	1.67	139	ns
ambient temperature	T_{amb}	in free air	-40	-	+125	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to VSS (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
ON resistance (peak)	$R_{ON(peak)}$	V_{is} =V_{DD} to V_{SS}; I_{SW} = 1000 uA	V_{DD} = 4.5 V	-	110	180	Ω
			V_{DD} = 6.0 V	-	95	160	Ω
			V_{DD} = 9.0 V	-	75	130	Ω
ON resistance (rail)	$R_{ON(rail)}$	V_{is} = V_{SS} or V_{DD} I_{SW} = 1000 uA	V_{DD} = 4.5 V	-	90	160	Ω
			V_{DD} = 6.0 V	-	80	140	Ω
			V_{DD} = 9.0 V	-	70	120	Ω
ON resistance mismatch between channels	ΔR_{ON}	V_{is} = V_{DD} to V_{SS}	V_{DD} = 4.5 V	-	9	-	Ω
			V_{DD} = 6.0 V	-	8	-	Ω
			V_{DD} = 9.0 V	-	6	-	Ω
AiP74HC4097							
HIGH-level input voltage	V_{IH}	V_{DD} = 4.5 V		3.15	2.4	-	V
		V_{DD} = 6.0 V		4.2	3.2	-	V
		V_{DD} = 9.0 V		6.3	4.7	-	V
LOW-level input voltage	V_{IL}	V_{DD} = 4.5 V		-	2.1	1.35	V
		V_{DD} = 6.0 V		-	2.8	1.80	V
		V_{DD} = 9.0 V		-	4.3	2.70	V
input leakage current	I_I	V_I = V_{DD} or V_{SS}	V_{DD} = 6.0 V	-	-	±0.1	uA
			V_{DD} = 9.0 V	-	-	±0.2	uA
OFF-state leakage current	$I_{S(OFF)}$	V_{DD}= 9.0 V; V_I= V_{IH} or V_{IL}; $\|V_{SW}\|$= V_{DD} - V_{SS}; see Figure 8	per channel	-	-	±0.1	uA
			all channels	-	-	±0.8	uA
ON-state leakage current	$I_{S(ON)}$	V_{DD}= 9.0 V; V_I= V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{DD} - V_{SS}; see Figure 9		-	-	±0.8	uA
supply current	I_{DD}	V_I = V_{DD} or V_{SS}; V_{is} = V_{SS} or V_{DD}; V_{os} = V_{DD} or V_{SS}	V_{DD} = 6.0 V	-	-	8.0	uA
			V_{DD} = 9.0 V	-	-	16.0	uA
input capacitance	C_I	-		-	3.5	-	pF
AiP74HCT4097							
HIGH-level input voltage	V_{IH}	V_{DD} = 4.5 V to 5.5 V		2.0	1.6	-	V
LOW-level input voltage	V_{IL}	V_{DD} = 4.5 V to 5.5 V		-	1.2	0.8	V
input leakage current	I_I	V_I = V_{DD} or V_{SS}; V_{DD} = 5.5 V		-	-	±0.1	uA

OFF-state leakage current	$I_{S(OFF)}$	V_{DD}= 5.5 V; V_I= V_{IH} or V_{IL}; $\|V_{SW}\|$= V_{DD} - V_{SS}; see Figure 8	per channel	-	-	±0.1	uA
			all channels	-	-	±0.8	uA
ON-state leakage current	$I_{S(ON)}$	V_{DD}= 5.5 V; V_I= V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{DD}-V_{SS}; see Figure 9		-	-	±0.8	uA
supply current	I_{DD}	V_I = V_{DD} or V_{SS}; V_{is} = V_{SS} or V_{DD}; V_{os} = V_{DD} or V_{SS}; V_{DD}=4.5 V to 5.5V		-	-	8.0	uA
additional supply current	ΔI_{DD}	per input pin; V_I = V_{DD}-2.1V; other inputs at V_{DD} or V_{SS}; V_{DD} = 4.5 V to 5.5 V	pin $\bar{E}$	-	60	216	uA
			pin An	-	50	180	uA
input capacitance	C_I	-		-	3.5	-	pF

Note:

[1] V_I= V_{IH} or V_{IL}; for test circuit see Figure 6.

[2] V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

[3] V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃~125℃, voltages are reference to V_{SS} (ground=0V), unless otherwise specified, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
ON resistance (peak)	$R_{ON(peak)}$	V_{is} =V_{DD} to V_{SS}; I_{SW} = 1000 uA	V_{DD} = 4.5 V	-	-	270	Ω
			V_{DD} = 6.0 V	-	-	240	Ω
			V_{DD} = 9.0 V	-	-	195	Ω
ON resistance (rail)	$R_{ON(rail)}$	V_{is} = V_{SS} or V_{DD} I_{SW} = 1000 uA	V_{DD} = 4.5 V	-	-	240	Ω
			V_{DD} = 6.0 V	-	-	210	Ω
			V_{DD} = 9.0 V	-	-	180	Ω
ON resistance mismatch between channels	ΔR_{ON}	V_{is} = V_{DD} to V_{SS}	V_{DD} = 4.5 V	-	-	-	Ω
			V_{DD} = 6.0 V	-	-	-	Ω
			V_{DD} = 9.0 V	-	-	-	Ω
AiP74HC4097							
HIGH-level input voltage	V_{IH}	V_{DD} = 4.5 V		3.15	-	-	V
		V_{DD} = 6.0 V		4.2	-	-	V
		V_{DD} = 9.0 V		6.3	-	-	V
LOW-level input voltage	V_{IL}	V_{DD} = 4.5 V		-	-	1.35	V
		V_{DD} = 6.0 V		-	-	1.80	V

		V_{DD} = 9.0 V		-	-	2.70	V
input leakage current	I_I	V_I = V_{DD} or V_{SS}	V_{DD} = 6.0 V	-	-	±1.0	uA
			V_{DD} = 9.0 V	-	-	±2.0	uA
OFF-state leakage current	$I_{S(OFF)}$	V_{DD}= 9.0 V; V_I= V_{IH} or V_{IL}; $\|V_{SW}\|$= V_{DD} - V_{SS}; see Figure 8	per channel	-	-	±1.0	uA
			all channels	-	-	±8.0	uA
ON-state leakage current	$I_{S(ON)}$	V_{DD}= 9.0 V; V_I= V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{DD} - V_{SS}; see Figure 9		-	-	±8.0	uA
supply current	I_{DD}	V_I = V_{DD} or V_{SS}; V_{is} = V_{SS} or V_{DD}; V_{os} = V_{DD} or V_{SS}	V_{DD} = 6.0 V	-	-	80.0	uA
			V_{DD} = 9.0 V	-	-	160.0	uA
input capacitance	C_I	-		-	-	-	pF
AiP74HCT4097							
HIGH-level input voltage	V_{IH}	V_{DD} = 4.5 V to 5.5 V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{DD} = 4.5 V to 5.5 V		-	-	0.8	V
input leakage current	I_I	V_I = V_{DD} or V_{SS}; V_{DD} = 5.5 V		-	-	±1.0	uA
OFF-state leakage current	$I_{S(OFF)}$	V_{DD}= 5.5V; V_I= V_{IH} or V_{IL}; $\|V_{SW}\|$=V_{DD}-V_{SS}; see Figure 8	per channel	-	-	±1.0	uA
			all channels	-	-	±8.0	uA
ON-state leakage current	$I_{S(ON)}$	V_{DD}= 5.5 V; V_I= V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{DD}-V_{SS}; see Figure 9		-	-	±8.0	uA
supply current	I_{DD}	V_I = V_{DD} or V_{SS}; V_{is} = V_{SS} or V_{DD}; V_{os} = V_{DD} or V_{SS}; V_{DD}=4.5 V to 5.5V		-	-	80.0	uA
additional supply current	ΔI_{DD}	per input; V_I = V_{DD} - 2.1V; other inputs at V_{DD} or V_{SS}; V_{DD} = 4.5 V to 5.5 V	pin $\bar{E}$	-	-	270	uA
			pin An	-	-	225	uA
input capacitance	C_I	-		-	-	-	pF

Note:

[1] $V_I = V_{IH}$ or V_{IL}; for test circuit see Figure 6.

[2] V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

[3] V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

3.3.3、AC Characteristics 1

(T_{amb}=25℃, V_{SS} = 0 V; $t_r = t_f$= 6 ns; C_L= 50 pF; unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC4097							
propagation delay	t_{pd}	nYn to nZ; see Figure 10[1][2]	V_{DD} = 4.5 V	-	9	15	ns
			V_{DD} = 6.0 V	-	7	13	ns
			V_{DD} = 9.0 V	-	5	9	ns
		nZ to nYn; see Figure 10[1][2]	V_{DD} = 4.5 V	-	6	12	ns
			V_{DD} = 6.0 V	-	5	10	ns
			V_{DD} = 9.0 V	-	4	8	ns
turn-off time	t_{off}	$\overline{E}$ to nYn; see Figure 11[3]	V_{DD} = 4.5 V	-	27	50	ns
			V_{DD} = 5.0 V; C_L = 15 pF	-	27	-	ns
			V_{DD} = 6.0 V	-	22	43	ns
			V_{DD} = 9.0 V	-	20	38	ns
		An to nYn; see Figure 11[3]	V_{DD} = 4.5 V	-	30	50	ns
			V_{DD} = 5.0 V; C_L = 15 pF	-	29	-	ns
			V_{DD} = 6.0 V	-	24	43	ns
			V_{DD} = 9.0 V	-	21	38	ns
		$\overline{E}$ to nZ; see Figure 11[3]	V_{DD} = 4.5 V	-	31	55	ns
			V_{DD} = 6.0 V	-	25	47	ns
			V_{DD} = 9.0 V	-	24	42	ns
		An to nZ; see Figure 11[3]	V_{DD} = 4.5 V	-	34	58	ns
			V_{DD} = 6.0 V	-	27	47	ns
			V_{DD} = 9.0 V	-	25	45	ns
turn-on time	t_{on}	$\overline{E}$ to nYn; see Figure 11[3]	V_{DD} = 4.5 V	-	29	55	ns
			V_{DD} = 5.0 V; C_L = 15 pF	-	26	-	ns
			V_{DD} = 6.0 V	-	23	47	ns
			V_{DD} = 9.0 V	-	17	42	ns
		An to nYn; see Figure 11[3]	V_{DD} = 4.5 V	-	32	60	ns
			V_{DD} = 5.0 V; C_L = 15 pF	-	29	-	ns
			V_{DD} = 6.0 V	-	26	51	ns

			V_{DD} = 9.0 V	-	18	45	ns
		$\overline{E}$ to nZ; see Figure 11[3]	V_{DD} = 4.5 V	-	31	55	ns
			V_{DD} = 6.0 V	-	25	47	ns
			V_{DD} = 9.0 V	-	18	42	ns
		An to nZ; see Figure 11[3]	V_{DD} = 4.5 V	-	34	60	ns
			V_{DD} = 6.0 V	-	27	51	ns
			V_{DD} = 9.0 V	-	19	45	ns
power dissipation capacitance	C_{PD}	per switch; V_I = V_{SS} to V_{DD}[4]		-	29	-	pF
AiP74HCT4097							
propagation delay	t_{pd}	nYn to nZ; see Figure 10[1][2]	V_{DD} = 4.5 V	-	9	15	ns
		nZ to nYn; see Figure 10[1][2]	V_{DD} = 4.5 V	-	6	12	ns
turn-off time	t_{off}	$\overline{E}$ to nYn; see Figure 11[3]	V_{DD} = 4.5 V	-	26	55	ns
			V_{DD} = 5.0 V; C_L = 15 pF	-	26	-	ns
		An to nYn; see Figure 11[3]	V_{DD} = 4.5 V	-	31	55	ns
			V_{DD} = 5.0 V; C_L = 15 pF	-	30	-	ns
		$\overline{E}$ to nZ; see Figure 11[3]	V_{DD} = 4.5 V	-	30	60	ns
		An to nZ; see Figure 11[3]	V_{DD} = 4.5 V	-	35	60	ns
turn-on time	t_{on}	$\overline{E}$ to nYn; see Figure 11[3]	V_{DD} = 4.5 V	-	32	60	ns
			V_{DD} = 5.0 V; C_L = 15 pF	-	32	-	ns
		An to nYn; see Figure 10[3]	V_{DD} = 4.5 V	-	35	60	ns
			V_{DD} = 5.0 V; C_L = 15 pF	-	33	-	ns
		$\overline{E}$ to nZ; see Figure 11[3]	V_{DD} = 4.5 V	-	38	65	ns
		An to nZ; see Figure 11[3]	V_{DD} = 4.5 V	-	38	65	ns
power dissipation	C_{PD}	per switch; V_I = V_{SS} to V_{DD}-1.5V[4]		-	29	-	pF

capacitance						

Note:

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] Due to higher nZ terminal capacitance (16 switches versus 1) the delay figures to the nZ terminal are higher than those to the nYn terminal.

[3] t_{on} is the same as t_{PZH} and t_{PZL}.

[4] t_{off} is the same as t_{PHZ} and t_{PLZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D = C_{PD} \times V_{DD}^2 \times f_i + \Sigma\{(C_L + C_{SW}) \times V_{DD}^2 \times f_O\}$ where:

f_i = input frequency in MHz;

f_O = output frequency in MHz;

$\Sigma\{(C_L + C_{SW}) \times V_{DD}^2 \times f_O\}$ = sum of outputs;

C_L = output load capacitance in pF;

C_{SW} = switch capacitance in pF;

V_{DD} = supply voltage in V.

[5] For test circuit see Figure 12.

[6] V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

[7] V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

3.3.4、AC Characteristics 2

(T_{amb}= -40℃~+125℃; V_{SS} = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC4097							
propagation delay	t_{pd}	nYn to nZ; see Figure 10[1][2]	V_{DD} = 4.5 V	-	-	22	ns
			V_{DD} = 6.0 V	-	-	19	ns
			V_{DD} = 9.0 V	-	-	14	ns
		nZ to nYn; see Figure 10[1][2]	V_{DD} = 4.5 V	-	-	18	ns
			V_{DD} = 6.0 V	-	-	15	ns
			V_{DD} = 9.0 V	-	-	12	ns
turn-off time	t_{off}	$\overline{E}$ to nYn; see Figure 10[3]	V_{DD} = 4.5 V	-	-	75	ns
			V_{DD} = 5.0 V; C_L = 15 pF	-	-	-	ns
			V_{DD} = 6.0 V	-	-	64	ns
			V_{DD} = 9.0 V	-	-	57	ns
		An to nYn; see Figure 11[3]	V_{DD} = 4.5 V	-	-	75	ns
			V_{DD} = 5.0 V; C_L = 15 pF	-	-	-	ns
			V_{DD} = 6.0 V	-	-	64	ns
			V_{DD} = 9.0 V	-	-	57	ns
		$\overline{E}$ to nZ; see Figure 11[3]	V_{DD} = 4.5 V	-	-	83	ns
			V_{DD} = 6.0 V	-	-	71	ns
			V_{DD} = 9.0 V	-	-	63	ns
		An to nZ; see Figure 11[3]	V_{DD} = 4.5 V	-	-	87	ns
			V_{DD} = 6.0 V	-	-	74	ns
			V_{DD} = 9.0 V	-	-	68	ns
turn-on time	t_{on}	$\overline{E}$ to nYn; see Figure 11[3]	V_{DD} = 4.5 V	-	-	83	ns
			V_{DD} = 5.0 V; C_L = 15 pF	-	-	-	ns
			V_{DD} = 6.0 V	-	-	71	ns
			V_{DD} = 9.0 V	-	-	63	ns
		An to nYn; see Figure 11[3]	V_{DD} = 4.5 V	-	-	90	ns
			V_{DD} = 5.0 V; C_L = 15 pF	-	-	-	ns
			V_{DD} = 6.0 V	-	-	77	ns
			V_{DD} = 9.0 V	-	-	68	ns
		$\overline{E}$ to nZ; see Figure 11[3]	V_{DD} = 4.5 V	-	-	83	ns
			V_{DD} = 6.0 V	-	-	71	ns

			V_{DD} = 9.0 V	-	-	63	ns
		An to nZ; see Figure 11[3]	V_{DD} = 4.5 V	-	-	90	ns
			V_{DD} = 6.0 V	-	-	77	ns
			V_{DD} = 9.0 V	-	-	68	ns
power dissipation capacitance	C_{PD}	per switch; V_I = V_{SS} to V_{DD}[4]		-	-	-	pF
AiP74HCT4097							
propagation delay	t_{pd}	nYn to nZ; see Figure 10[1][2]	V_{DD} = 4.5 V	-	-	22	ns
		nZ to nYn; see Figure 10[1][2]	V_{DD} = 4.5 V	-	-	18	ns
turn-off time	t_{off}	$\overline{E}$ to nYn; see Figure 11[3]	V_{DD} = 4.5 V	-	-	83	ns
			V_{DD} = 5.0 V; C_L = 15 pF	-	-	-	ns
		An to nYn; see Figure 11[3]	V_{DD} = 4.5 V	-	-	83	ns
			V_{DD} = 5.0 V; C_L = 15 pF	-	-	-	ns
		$\overline{E}$ to nZ; see Figure 11[3]	V_{DD} = 4.5 V	-	-	90	ns
		An to nZ; see Figure 11[3]	V_{DD} = 4.5 V	-	-	90	ns
turn-on time	t_{on}	$\overline{E}$ to nYn; see Figure 11[3]	V_{DD} = 4.5 V	-	-	90	ns
			V_{DD} = 5.0 V; C_L = 15 pF	-	-	-	ns
		An to nYn; see Figure 11[3]	V_{DD} = 4.5 V	-	-	90	ns
			V_{DD} = 5.0 V; C_L = 15 pF	-	-	-	ns
		$\overline{E}$ to nZ; see Figure 11[3]	V_{DD} = 4.5 V	-	-	98	ns
		An to nZ; see Figure 11[3]	V_{DD} = 4.5 V	-	-	98	ns
power dissipation capacitance	C_{PD}	per switch; V_I = V_{SS} to V_{DD}-1.5V[4]		-	-	-	pF

Note:

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] Due to higher nZ terminal capacitance (16 switches versus 1) the delay figures to the nZ terminal are higher than those to the nYn terminal.

[3] t_{on} is the same as t_{PZH} and t_{PZL}.

[4] t_{off} is the same as t_{PHZ} and t_{PLZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D = C_{PD} \times V_{DD}^2 \times f_i + \Sigma\{(C_L + C_{SW}) \times V_{DD}^2 \times f_O\}$ where:

f_i = input frequency in MHz;

f_O = output frequency in MHz;

$\Sigma\{(C_L + C_{SW}) \times V_{DD}^2 \times f_O\}$ = sum of outputs;

C_L = output load capacitance in pF;

C_{SW} = switch capacitance in pF;

V_{DD} = supply voltage in V.

[5] For test circuit see Figure 12.

[6] V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

[7] V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

3.3.5、AC Characteristics 3

(T_{amb}= 25°C; V_{SS} = 0V; C_L=50pF; recommended conditions and typical values.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
total harmonic distortion	THD	f_i = 1 kHz; C_L= 50pF; R_L = 10 kΩ; see Figure 13	V_{DD} = 4.5 V; $V_{is(p-p)}$= 4.0 V	-	0.04	-	%
			V_{DD} = 9.0 V; $V_{is(p-p)}$= 8.0 V	-	0.02	-	%
		f_i = 10 kHz; C_L= 50pF; R_L = 10 kΩ; see Figure 13	V_{DD} = 4.5 V; $V_{is(p-p)}$= 4.0 V	-	0.12	-	%
			V_{DD} = 9.0 V; $V_{is(p-p)}$= 8.0 V	-	0.06	-	%
isolation (OFF-state)	α_{iso}	R_L= 600 Ω; C_L= 50pF; see Figure 14	V_{DD} = 4.5 V; [1]	-	-50	-	dB
			V_{DD} = 9.0 V; [1]	-	-50	-	dB
-3dB frequency response	$f_{(-3dB)}$	R_L = 50 Ω; C_L= 10pF; see Figure 15	V_{DD} = 4.5 V; [2]	-	90	-	MHz
			V_{DD} = 9.0 V; [2]	-	100	-	MHz
switch capacitance	C_{SW}	independent pins Y		-	5	-	pF
		common pin Z		-	45	-	pF

Note：

[1] Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).

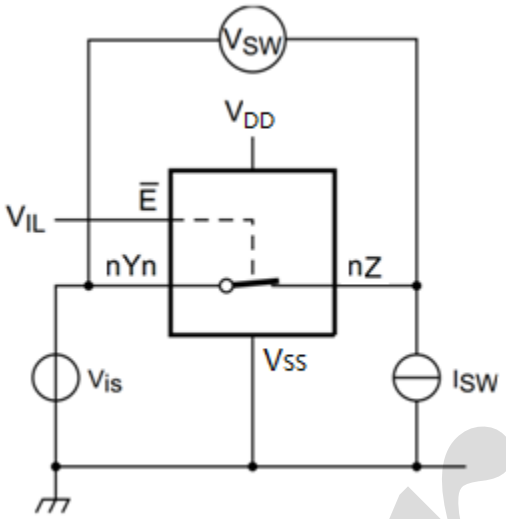
[2] Adjust input voltage V_{is} to 0 dBm level at V_{os} for f_i = 1 MHz (0 dBm = 1 mW into 50Ω). After set-up, f_i is increased to obtain a reading of -3dB at V_{os}.

[3] V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

[4] V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

4、Testing Circuit

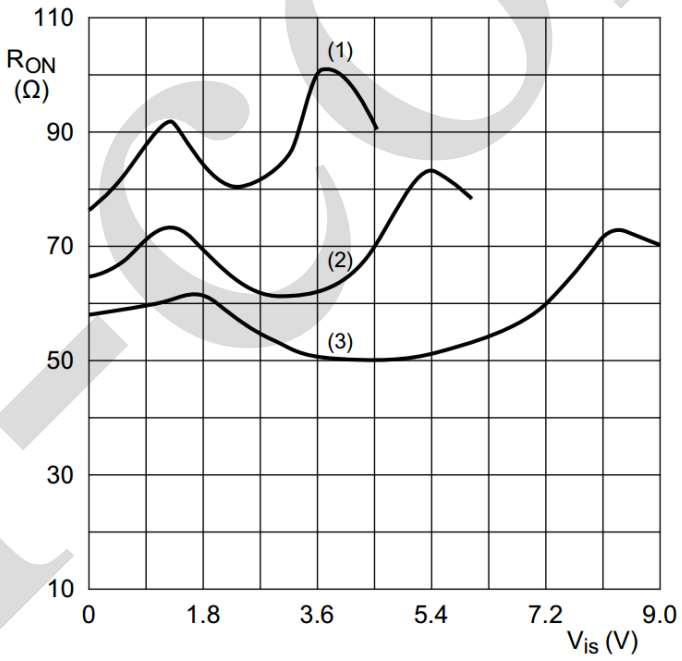
4.1、DC Testing Circuit 1



V_{is} = 0V to V_{CC}

$R_{ON} = V_{SW}/I_{SW}$

Figure 6. Test circuit for measuring R_{ON}



V_{is} = 0V to V_{DD}

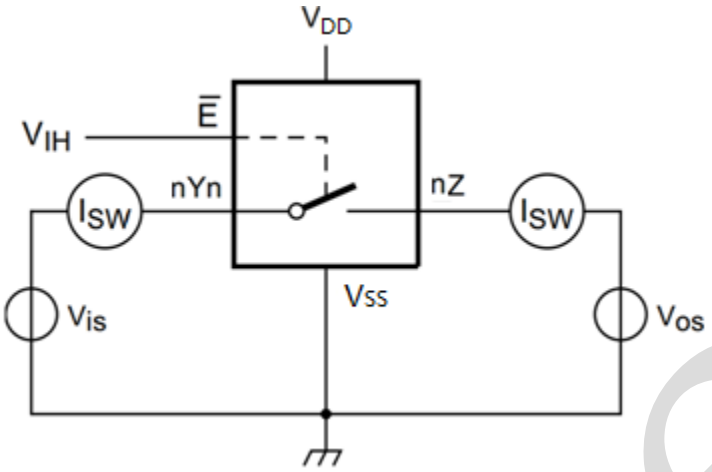
(1)V_{DD} = 4.5V

(2)V_{DD} = 6.0V

(3)V_{DD} = 9.0V

Figure 7. Typical R_{ON} as a function of input voltage V_{is}

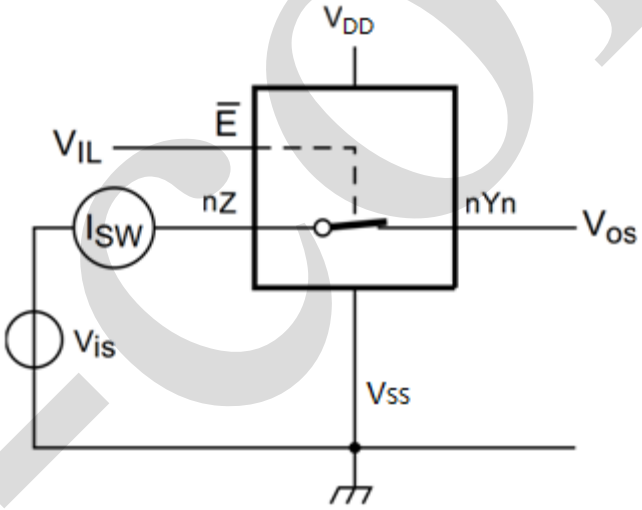
4.2、DC Testing Circuit 2



V_{is}= V_{DD} and V_{os}= V_{SS}

V_{is}= V_{SS} and V_{os}= V_{DD}

Figure 8. Test circuit for measuring OFF-state leakage current



V_{is}= V_{DD} and V_{os}= open

V_{is}= V_{SS} and V_{os}= open

Figure 9. Test circuit for measuring ON-state leakage current

4.3、AC Testing Waveforms

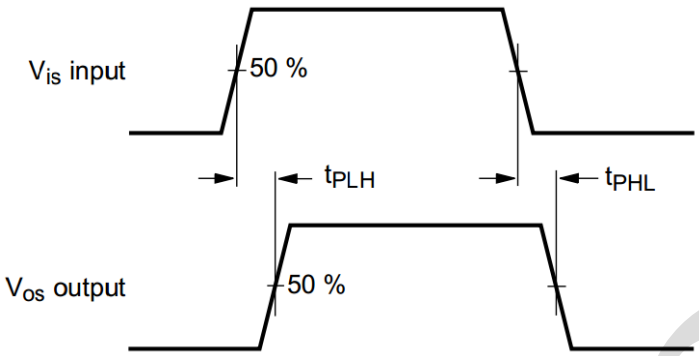


Figure 10. Input (V_{is}) to output (V_{os}) propagation delays

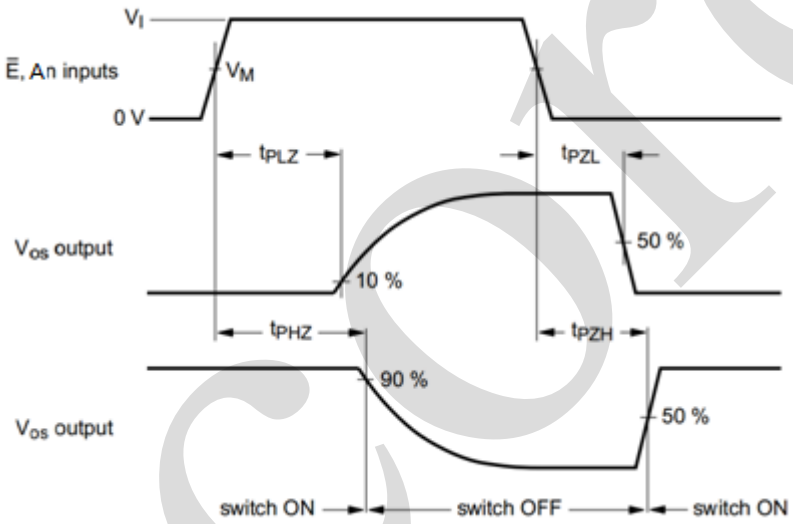


Figure 11. Turn-on and turn-off times

4.4、Measurement Points

Type	V_I	V_M
AiP74HC4097	V_{DD}	$0.5V_{DD}$
AiP74HCT4097	3.0V	1.3V

4.5、AC Testing Circuit 1

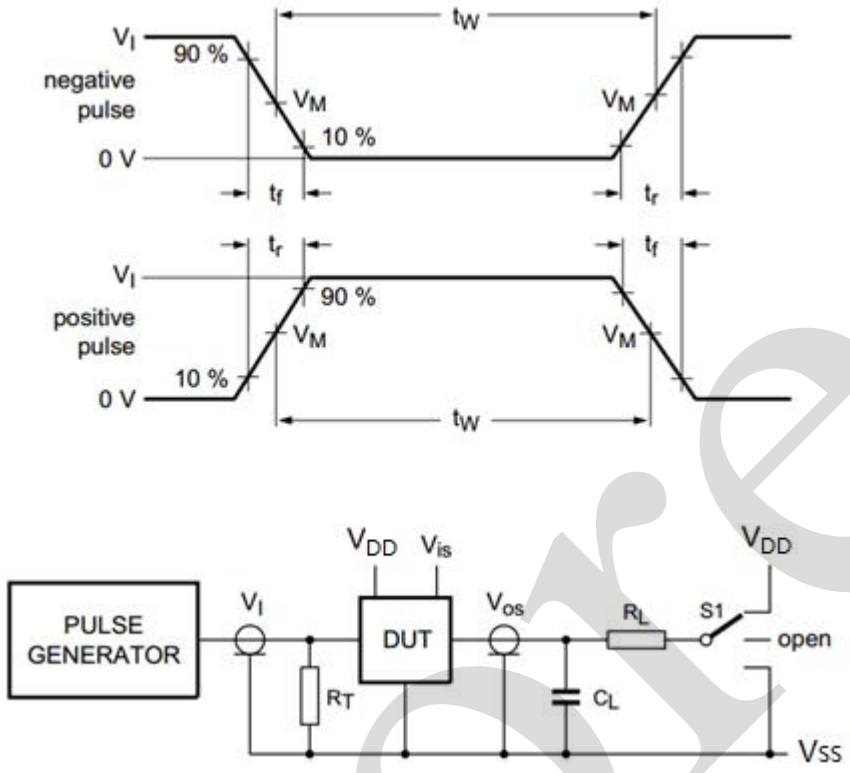


Figure 12. Test circuit for measuring switching times

Definitions for test circuit:

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

S1 = Test selection switch.

4.6、Test Data

Test	Input				Output		S1 position
	Control $\overline{E}$	Address An	Switch nYn (nZ)	t_r, t_f	Switch nZ (nYn)		
	V_I[1]	V_I[1]	V_{is}		C_L	R_L	
t_{PHL},t_{PLH}	V_{SS}	V_{SS} or V_{DD}	V_{SS} to V_{DD}	6ns	50pF	-	open
t_{PHZ},t_{PZH}	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V_{DD}	6ns	50pF,15pF	1kΩ	V_{SS}
t_{PLZ},t_{PZL}	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V_{SS}	6ns	50pF,15pF	1kΩ	V_{DD}

Note:

[1] For AiP74HCT4097: maximum input voltage V_I= 3.0 V.

4.7、AC Testing Circuit 2

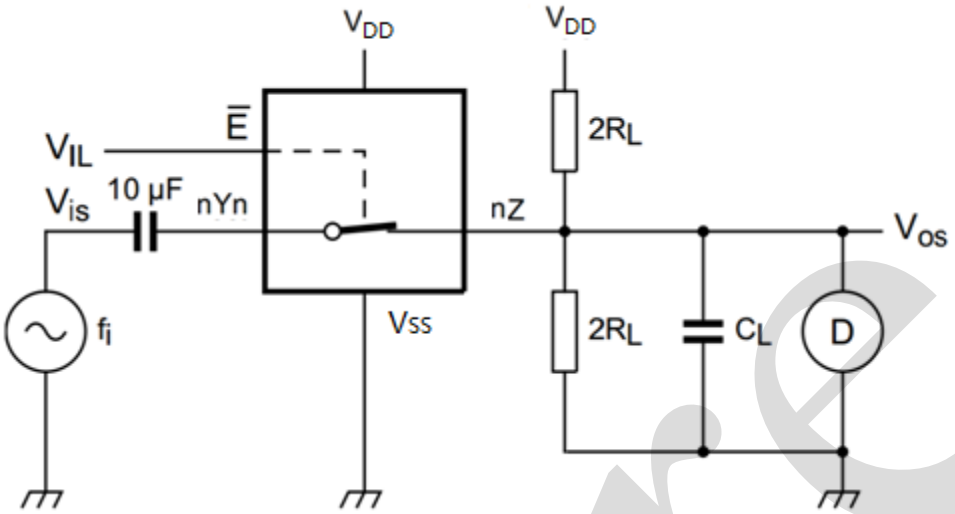
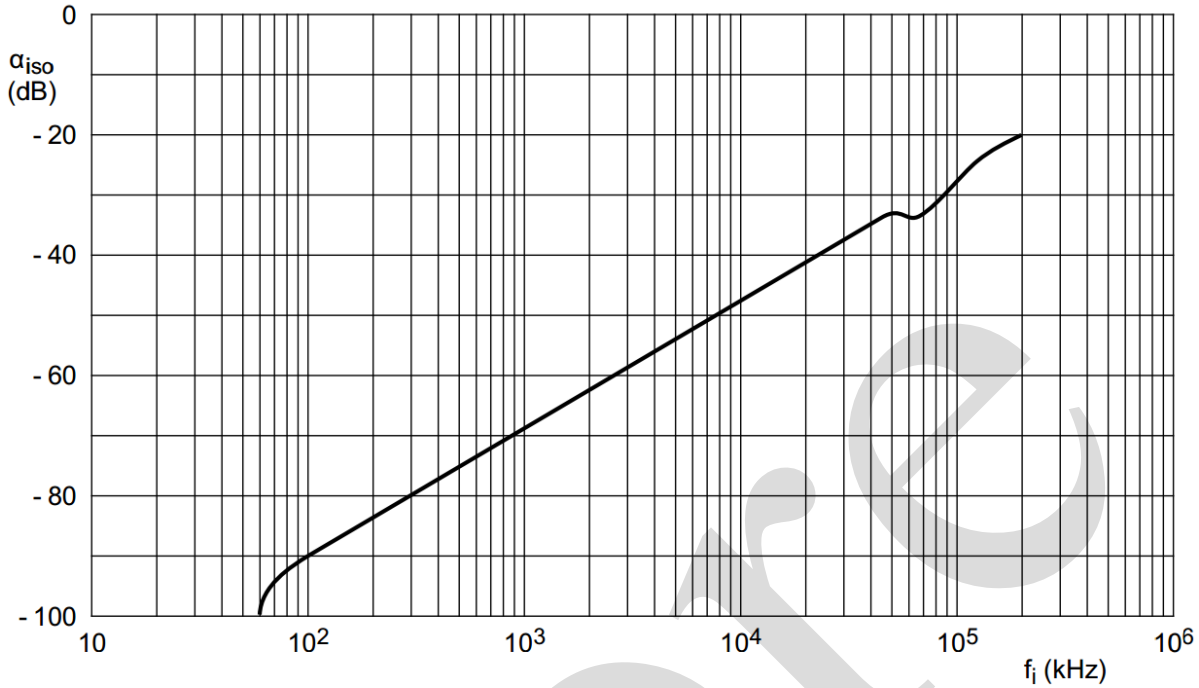
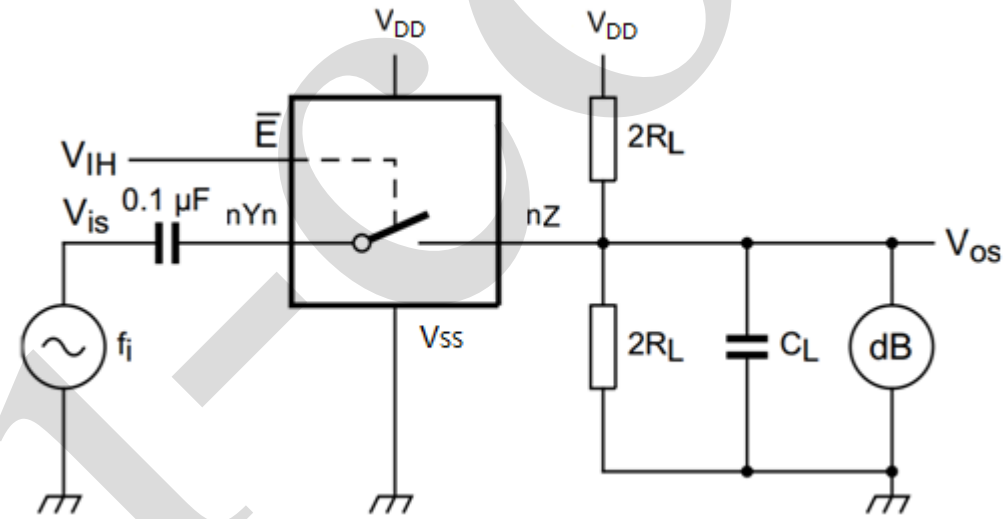


Figure 13. Test circuit for measuring total harmonic distortion



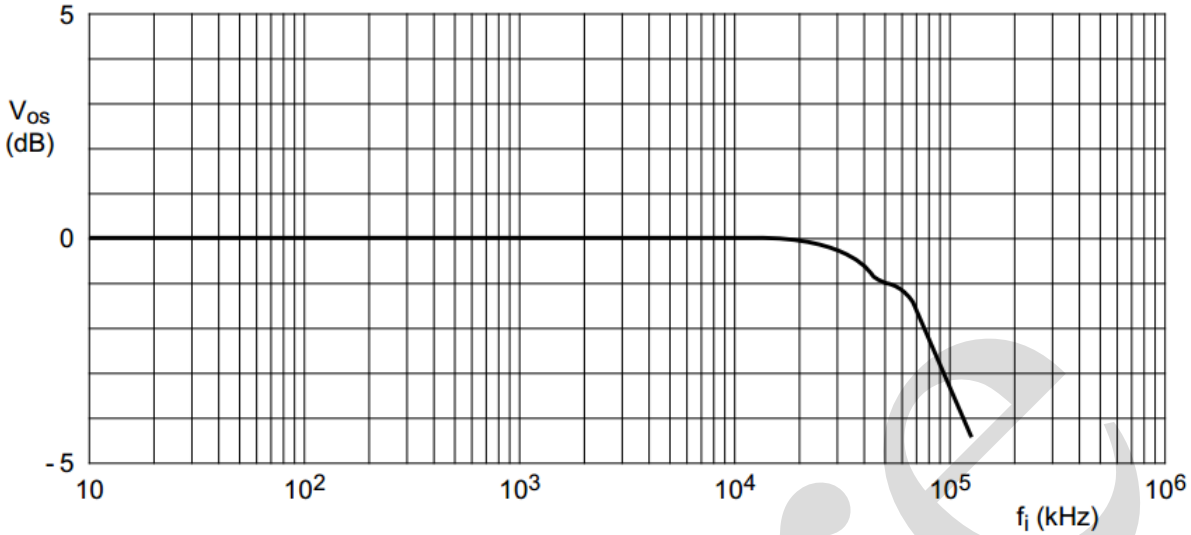
a. Isolation (OFF-state)



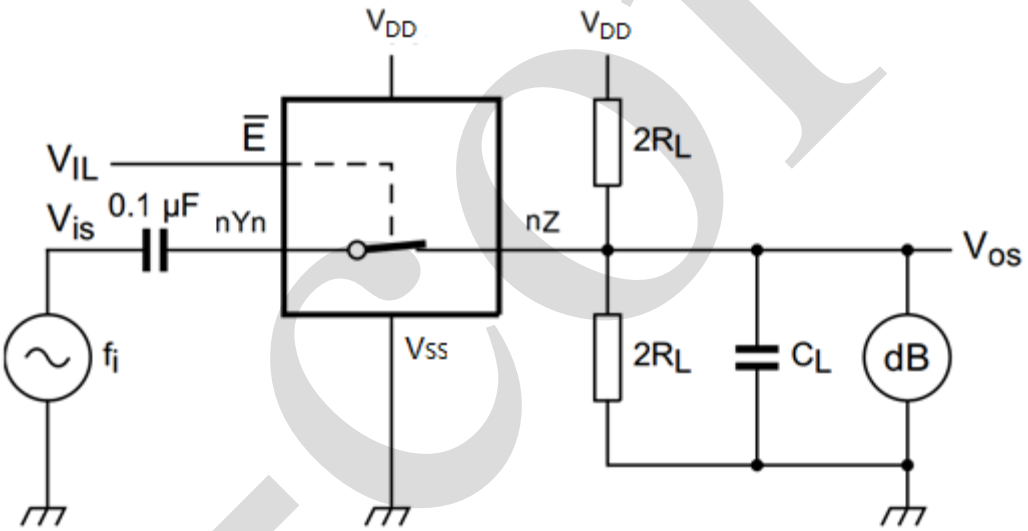
b. Test circuit

V_{DD} = 4.5 V; V_{SS} = 0 V; R_L = 600 Ω; R_{source} = 1 kΩ.

Figure 14. Isolation (OFF-state) as a function of frequency



a. Typical -3 dB frequency response



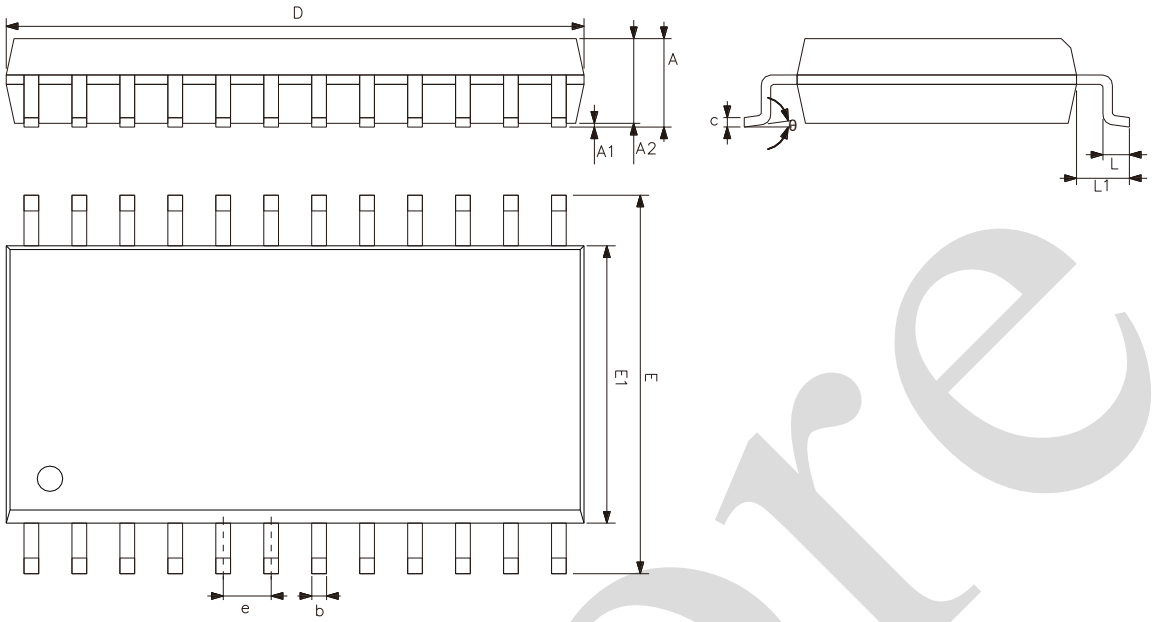
b. Test circuit

V_{DD} = 4.5 V; V_{SS} = 0 V; R_L = 50Ω; R_{source} = 1 kΩ.

Figure 15. -3 dB frequency response

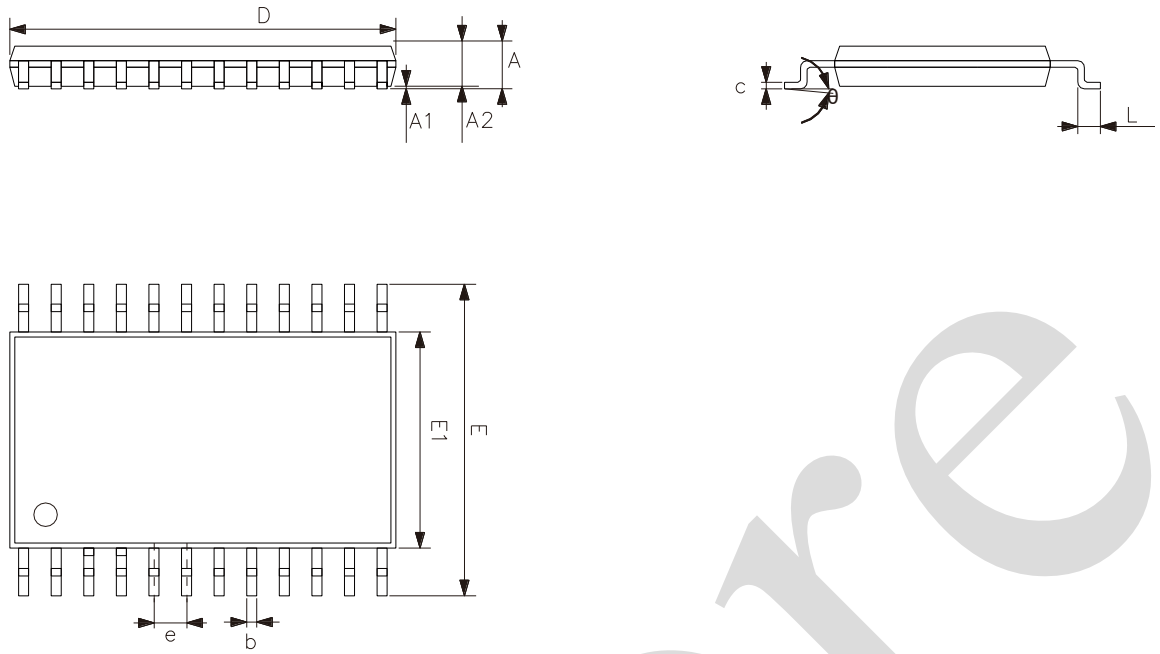
5、Package Information

5.1、SOP24



Symbol	Dimensions (mm)	
	Min.	Max.
A	2.35	2.65
A1	0.10	0.30
A2	2.13	2.44
b	0.39	0.47
c	0.25	0.30
D	15.19	15.55
E	10.10	10.57
E1	7.40	7.62
e	1.27	
L	0.41	1.00
L1	1.30	1.50
θ	0°	8°

5.3、TSSOP24



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.20	6.60
E1	4.30	4.50
e	0.65	
L	0.45	0.75
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notion

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

This information is using to the reference only, the company is not responsible for any loss；

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.